UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,545	03/24/2004	Mitsuaki Osame	12732-223001 / US7068/714	3777

26171 7590 01/04/2011

FISH & RICHARDSON P.C. (DC)
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
BECK, ALEXANDER S	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
01/04/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/807,545	OSAME ET AL.	
	Examiner	Art Unit	
	Alexander S. Beck	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,15,17,28,32,34-40,43-47,50-55 and 58-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,15,17,28,32,34-40,43-47,50-55 and 58-75* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 November 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ ~~Notice of References Cited (PTO-892)~~
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/1/2010*.
4) ☐ ~~Interview Summary (PTO-413)~~ Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

I. RESPONSE TO AMENDMENT

Acknowledgment is made of the amendment filed October 22, 2010 ("Amend."), which the rejections of the claims are traversed. Claims 3, 15, 17, 28, 32, 34-40, 43-47, 50-55, and 58-75 are currently pending and an Office action on the merits follows.

II. INFORMATION DISCLOSURE STATEMENT

The information disclosure statement filed November 1, 2010, has been acknowledged and considered by the examiner. An initialed copy of the PTO-1449 is included in this correspondence.

III. DOUBLE PATENTING

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claims 3, 15, 17, 28, 32, 34-40, 43-47, 50-55, and 58-75 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3, and 4 of U.S. Patent No. *7,122,969 to Fukumoto et al. ("'969 Patent")* in view of *U.S. Patent Pub. No. 2001/0002703 by Koyama ("Koyama")*

For example, comparing the present application with the '934 Patent as below:

present application (claim 61)	'969 Patent (claims 1, 3, and 4)
An element substrate comprising:	A light emitting device comprising: (claim 1, l. 1)
a first power line; a second power line; a scan line; a signal line; a pixel electrode; a first transistor; a second transistor; and a third transistor,	a scan line; a signal line intersecting with the scan line; a first to a n-th power supply lines ... a light emitting element; a first transistor ... a second transistor (claim 1, ll. 2-13)
wherein one of a source and a drain of the first transistor is connected to the pixel electrode, wherein one of a source and drain of the second transistor is connected to the other of the source and the drain of the first transistor, wherein the other of the source and the drain of the second transistor is connected to the first power line	wherein the first power source, the first transistor, the second transistor, and the light emitting element are connected in series (claim 1, ll. 14-16)
wherein a gate of the first transistor is connected to the second power line,	wherein a first region of a gate electrode of the first transistor is electrically connected to a k-th power supply line, wherein a

	second region of the gate electrode of the first transistor is electrically connected to a (k+1)-th power supply line (claim 1, ll. 17-22)
wherein one of a source and a drain of the third transistor is connected to a gate electrode of the second transistor, wherein the other of the source and the drain of the third transistor is connected to the signal line, wherein a gate electrode of the third transistor is connected to the scan line,	
wherein the first transistor has a channel length longer than a channel width, and the second transistor has a channel length equal to or shorter than a channel width, and	wherein a channel length of the first transistor is longer than its channel width, and a channel length of the second transistor is equal to or shorter than its channel width (claim 3, ll. 1-5)
wherein a ratio of the channel length of the channel width of the first transistor is 5 or more.	a ratio of the channel length to the channel width of the first transistor is five or more (claim 4, ll. 1-3)

The '969 Patent does not disclose expressly a third transistor wherein one of a source and a drain of the third transistor is connected to a gate electrode of the second transistor, wherein the other of the source and the drain of the third transistor is connected to the signal line, wherein a gate electrode of the third transistor is connected to the scan line, as claimed.

Koyama discloses a light emitting device a third transistor (Koyama, 105; Fig. 3) wherein one of a source and a drain of the third transistor is connected to a gate electrode of the second transistor (Koyama, 109; Fig. 3), wherein the other of the source and the drain of the third transistor is connected to the signal line (Koyama, 107; Fig. 3), wherein a gate electrode of the third transistor is connected to the scan line (Koyama, 106; Fig. 3). At the time the invention was made it would have been obvious to one having ordinary skill in the art to modify the '969 Patent such that the third transistor was connected as taught by Koyama. As one of ordinary skill in the art would appreciate, the

suggestion/motivation for doing so would have been to control the input of the video signal to the pixel.

2. Claims 3, 15, 17, 28, 32, 34-40, 43-47, 50-55, and 58-75 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 11, 14, and 15 of U.S. Patent No. *7,141,934 to Osame et al. ("'934 Patent")* in view of U.S. Patent Pub. No. 2001/0002703 by Koyama

For example, comparing the present application with the '934 Patent as below:

present application (claim 61)	'934 Patent (claims 11, 14, and 15)
An element substrate comprising:	A light emitting device comprising: (claim 11, l. 2)
a first power line; a second power line; a scan line; a signal line; a pixel electrode; a first transistor; a second transistor; and a third transistor,	a light emitting element provided in a pixel; a first transistor … a second transistor … a third transistor …a first power supply and a second power supply (claim 11, ll. 2-12)
wherein one of a source and a drain of the first transistor is connected to the pixel electrode, wherein one of a source and drain of the second transistor is connected to the other of the source and the drain of the first transistor, wherein the other of the source and the drain of the second transistor is connected to the first power line	wherein the light emitting element is connected in series to the first transistor and the second transistor between a first power supply and a second power supply (claim 11, ll. 10-12)
wherein a gate of the first transistor is connected to the second power line,	a gate electrode of the first transistor is connected to the first power supply (claim 11, ll. 13-14)
wherein one of a source and a drain of the third transistor is connected to a gate electrode of the second transistor, wherein the other of the source and the drain of the third transistor is connected to the signal line, wherein a gate electrode of the third transistor is connected to the scan line,	
wherein the first transistor has a channel length longer than a channel width, and the second transistor has a channel length equal	wherein a channel length of the first transistor is longer than its channel width, and a channel length of the second

to or shorter than a channel width, and	transistor is equal to or shorter than its channel width (claim 14, ll. 1-4)
wherein a ratio of the channel length of the channel width of the first transistor is 5 or more.	a ratio of the channel length to the channel width of the first transistor is five or more (claim 15, ll. 1-3)

The '934 Patent does not disclose expressly wherein one of a source and a drain of the third transistor is connected to a gate electrode of the second transistor, wherein the other of the source and the drain of the third transistor is connected to the signal line, wherein a gate electrode of the third transistor is connected to the scan line, as claimed.

Koyama discloses a light emitting device wherein one of a source and a drain of the third transistor (Koyama, 105; Fig. 3) is connected to a gate electrode of the second transistor (Koyama, 109; Fig. 3), wherein the other of the source and the drain of the third transistor is connected to the signal line (Koyama, 107; Fig. 3), wherein a gate electrode of the third transistor is connected to the scan line (Koyama, 106; Fig. 3). At the time the invention was made it would have been obvious to one having ordinary skill in the art to modify the '934 Patent such that the third transistor was connected as taught by Koyama. As one of ordinary skill in the art would appreciate, the suggestion/motivation for doing so would have been to control the input of the video signal to the pixel.

IV. RESPONSE TO ARGUMENTS

Applicant's arguments filed October 22, 2010, have been fully considered but they are not persuasive. Applicant argues that the nonstatutory obviousness-type double patenting rejections should be withdrawn in light of the various differences between the claimed language in the instant application and the claimed language in the '969 patent and the '934 patent

However, **a nonstatutory obviousness-type double patenting rejection is appropriate** where the conflicting claims are not identical, but at least one examined

application claim is **not patentably distinct** from the reference claim(s) **because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s)**. See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); and In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985).

Furthermore, in determining whether a nonstatutory basis exists for a double patenting rejection, the first question to be asked is — does any claim in the application define an invention that is **anticipated by, or is merely an obvious variation of**, an invention claimed in the patent? If the answer is yes, then an "obviousness-type" nonstatutory double patenting rejection may be appropriate. Obviousness-type double patenting requires rejection of an application claim when the claimed subject matter is **not patentably distinct** from the subject matter claimed in a commonly owned patent, or a non-commonly owned patent but subject to a joint research agreement as set forth in 35 U.S.C. 103(c)(2) and (3), when the issuance of a second patent would provide unjustified extension of the term of the right to exclude granted by a patent. See Eli Lilly & Co. v. Barr Labs., Inc., 251 F.3d 955, 58 USPQ2d 1869 (Fed. Cir. 2001); Ex parte Davis, 56 USPQ2d 1434, 1435-36 (Bd. Pat. App. & Inter. 2000).

Applicant specifically argues that claim 61 of the instant application recites that one power supply is connected to the gate of the first transistor, whereas claims 1, 3 and 4 of the '969 patent recite that two power supply lines are connected to the gate of the first transistor (see Amend. 2). However, in light of the discussion of nonstatutory obviousness-type double patenting above, examiner respectfully submits the argued limitation of claim 61 is **not patentably distinct** from the cited limitation in claims 1, 3 and 4 of the '969 patent because a gate of a transistor connected to two power supply lines is inclusive of a gate of a transistor connected to one power supply. Thus, the scope of protection sought in the instant application is encompassed by the scope of protection

granted in the '969 patent. For at least this reason, the nonstatutory obviousness-type double patenting rejection will be maintained.

Applicant specifically argues that the '934 patent does not disclose "a gate electrode of the first transistor is connected to a second power line," as recited in claims 3 and 36-38 of the instant application and "a gate electrode of the first transistor is connected to the second power line," as recited in claims 61 an 69 of the instant application (see Amend. 2-3). However, in light of the discussion of nonstatutory obviousness-type double patenting above, examiner respectfully submits the argued limitations are **not patentably distinct** from the cited limitations in the '934 patent because the claimed "first power supply" of the '934 patent is functionally equivalent to the claimed "second power line" in the instant application, e.g., both are connected to a gate of the first transistor. Thus, the scope of protection sought in the instant application is encompassed by the scope of protection granted in the '934 patent. For at least this reason, the nonstatutory obviousness-type double patenting rejection will be maintained.

Applicant specifically argues that the pixel electrode in the instant application is not connected in series to the first transistor and the second transistor between the first power line and the second power line as recited in the '934 patent, but rather the gate of the first transistor is connected to the second power line (see Amend. 3-4). However, in light of the discussion of nonstatutory obviousness-type double patenting above, examiner respectfully submits the argued limitations are **not patentably distinct** from the cited limitations in the '934 patent because the claimed "first power supply" of the '934 patent (which is connected to the gate of the first transistor) is functionally equivalent to the claimed "second power line" in the instant application, e.g., both are connected to a gate of the first transistor. Thus, the scope of protection sought in the instant application is encompassed by the scope of protection granted in the '934 patent. For at least this reason, the nonstatutory obviousness-type double patenting rejection will be maintained.

Applicant specifically argues that claims 3, 36 and 37 of the instant application recite that "the light-emitting element, the first transistor, and the second transistor are connected in series between a first power line and a counter electrode of the light-emitting element," and "a gate electrode of the first transistor is connected to a second power line" (see Amend. 4). However, in light of the discussion of nonstatutory obviousness-type double patenting above, examiner respectfully submits the argued limitations are **not patentably distinct** from the cited limitations in the '934 patent because the other of the two power supplies in the '934 patent is connected to a counter electrode of the light-emitting element, and therefore meets the claimed limitation of the instant application. Furthermore, the claimed "first power supply" of the '934 patent (which is connected to the gate of the first transistor) is functionally equivalent to the claimed "second power line" in the instant application, e.g., both are connected to a gate of the first transistor. Thus, the scope of protection sought in the instant application is encompassed by the scope of protection granted in the '934 patent. For at least this reason, the nonstatutory obviousness-type double patenting rejection will be maintained.

V. CONCLUSION

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander S. Beck whose telephone number is (571) 272-7765. The examiner can normally be reached on M-F, 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alexander S. Beck/ Dated: December 29, 2010
Primary Examiner, Art Unit 2629